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| **S.NO** | **COMPANY NAME** | **ELIGIBILITY CRITERIA** | **SELECTION PROCESS** | **SKILL SET** |
| **1.** | **Smart DV Technologies,**  **Bangalore.** | **(ECE branch only )   70% and above in SSC, HSC and UG – No standing arrears** | **Technical cum General Aptitude Test followed by personnel Interview rounds.** | **1.Digital Electronics 2.C & C++ programming 3.Verilog 4.microprocessor 5.Electronic device 6.Networking theory** |
| **2.** | **Caliber Interconnect Solutions, Coimbatore** | **1. Should have a aggregate of 70% of marks in academics and no standing backlogs.**  **2. Branch of Study : ECE, EEE and E&I & ME – (Applied Electronics, VLSI, Communication system or any electronics)**  **3. Should not have any other standing Job offers.** | **\* One written round comprises of technical & verbal/non-verbal aptitude**  **\* One Technical HR for those who are short listed in the written round** | **Microprocessor and Microcontroller,**  **Digital electronics,**  **RF Concepts,**  **Circuit Theory** |
| **3.** | **Jasmin Infotech, Chennai** | **70% in 10th, 12th & UG**  **Departments : ECE, EEE, EIE** |  | **Electronic circuits,**  **C programming, Digital electronics, DSP, Microprocessor and Microcontroller** |
| **4.** | **Data Patterns, Chennai** | **Aggregate of 70% & above in 10th, 12th and Graduation.**  **No standing arrears as on date. Good written and spoken communication skills is required.**  **Departments : ECE, EEE, EIE** | **Written test will be for 90 minutes ( 1 hour hardware technical and 30 minutes aptitude)** | **Basics of Electronics (Analog and Digital circuits), Microprocessor & Microcontroller, ADCs, DACs, Multiplexers, LIC, OPAMP, Transistor, Diode family.** |
| **5.** | **Syrma, Chennai** | **10th-Morethan80% 12th-Morethan80% B.E – More than CGPA of 7**  **(ECE branch only )** | **Round 1 :Technical & Aptitude Test (Objective type)**  **Round 2:Group Discussion**  **Round 3:Technical Interview**  **Round 4:HR Interview**  **Round 5:Panel Interview in Chennai Syrma** | **Motors, Generators concepts**  **Digital Electronics**  **BJT, CMOS**  **R,L,C concepts**  **Power supplies, Rectifiers**  **EMF concepts** |
| **6.** | **Tessolve semiconductors Pvt Ltd, Bangalore & Chennai** | **70% in 10th, 12th & UG**  **Departments : ECE, EEE** | **Online Technical Test**  **Technical Round**  **Final HR Interview** | **Linear Integrated Circuits**  1. Op-amp  2. Differentiator  3. Integrator.  4. Sample and Hold circuit  5. Clipper and clamper  6. Adder, subtractor  7. Comparator  8. Regulated Power supply circuits  **Digital Logic Circuits**  1. Flipflops  2. Registers  3. Counters  4. Half and full adder  5. Subtractor  6. Mux and demux  7. Encoder and decoder  **Circuit Thoery**  1. Resistance reduction in a network  2. Voltage division and Current division  3. RL, RLC, RC network  4. Filters (low pass, high pass, band pass, Band reject) |
| **7.** | Aspire System Drive | **65% and above from 10th, 12th and Degree.**  **Departments : All Circuit branches** | **Interview Process: ( Day 1)**  **Round 1:**  Written Test (Paper based- 1 hour)  **Interview Process: ( Day 2)**  **Round 2:**  Technical Interview – Level 1  **Round 3:**  Technical Interview – Level 2  **Round 4:** HR Round |  |
| **8.** | Silicon House | 1. **BE / B Tech / M Tech (CS, IT, ECE, EEE, EIE) with an Aggregate of min 55% and above in Class X, XII and 60% above in degree or equivalent.** 2. **Only Female Candidates are eligible** | 1. **Group Discussion** 2. **Written Test** 3. **Personal Interview** |  |
| **9.** | Cosmic Circuits, Bangalore | **65 % with no standing arrears.**  **Departments : ECE, EEE, EIE** | **Written aptitude Test  and Technical Rounds** |  |
| **10.** | **Broadcom, Bangalore** | **60% and above from 10th, 12th and Degree.**  **No standing arrears**  EEE,CSE,IT, ECE,EIE - eligible | **Written aptitude Test  and Technical Rounds** |  |
| **11** | **MBIT Wireless, Chennai** | **Departments : ECE, CSE, IT**  SSLC : Minimum 85% and above  HSC : Minimum 85% and above  U.G : 7.5 CGPA and above with no history of arrears | **Test Schedule for ECE Candidates:**   * Test1 (45 Minutes) - Electronics paper-1 * Test2 (45 Minutes) - Electronics paper-2 * Test3 (45 Minutes) - Electronics paper-3 * Test4 (45 Minutes) - C programming | **1.Digital Electronics 2.C & C++ programming 3.Verilog 4.Microprocessor 5.Electronic device 6.Networking theory** |
| **12** | **Sure Soft Systems, Puducherry** | **60% and above from 10th, 12th and Degree.**  **No standing arrears**  EEE,CSE,IT, ECE,EIE - eligible | **Written Technical Test**  **Technical Round**  **Final HR Interview** |  C expertise is a must.   Thorough knowledge of Microprocessors/Electronics is required.   Electrical & Electronic circuits.   Software Engineering Concepts and Testing. |
| **13** | **TVS Electronics** | **65 % with no standing arrears.**  **Departments : ECE, EEE, EIE** |          Written Test (Basic Electronics and Aptitude)           Face to Face (Technical and HR) |          Good Communication & Interest in Electronics / Customer Service.           Profiles from Electronics Background.           Regional Language expertise, in the place where they will be deputed. |
| **14** | **Robert Bosch, Coimbatore** | **B.E (ECE, EEE, Instrumentation)**  **75% in 10th, 12th & UG** | **Written Technical Test**  **Two Technical Rounds**  **Final HR Interview** |          Experience in Automotive domain or a similar domain           Good knowledge in Programming in 'C' for real-time embedded systems           Experience in tools like VSS, Clearcase, Clear Quest, In-circuit Debuggers           Experience in handling actuators and sensors interface/driver software development           Good knowledge of Software Development Life Cycle quality standards is a MUST           Knowledge of control systems / Power train and Model Based Dev tools (ASCET, Matlab/Simulink) would be an added advantage |
| **15** | **Cadence AMS Design INDIA Pvt Ltd.** | Eligibility                    : 7.0 CGPA and above  (No Standing Arrears)  Branches                     : B.E -ECE, EEE, EIE  Designation                 : Analog Physical Design  Engineer  Salary                    : 6.6 Lakhs per annum.  **Description of role of Analog Physical Design Engineer**   * Analog Physical Design is the job of converting the analog schematics (represented by components like MOS, R & C) into a physical view that maps to the masks that are used for manufacturing in the FAB. * The Physical Design has significant impact on the performance and the dependence has gone up significantly with advanced technologies. * Good understanding of the manufacturing technology, basic working knowledge of the analog circuits, and impact of the layout on circuit performance will be a key. * The typical kind of blocks that we work on are ADC, DAC, PLL, Oscillator & High Speed SerDes etc. | 1. Pre placement talk  2. Written Test (90 mins)  3. Technical Round -30 min (approx) per person. | **written test would have aptitude and technical questions (Mostly Circuit theory, Analog and digital electronics)** |

**Some other Core industries, our Aluminums working are**

* **NXP Semiconductors, Bangalore**
* **INTEL, Bangalore**
* **Huawei, Bangalore**
* **Ansaldo STS, Bangalore**
* **TVM Signalling and Transportation Systems Private Limited (TSTS), Bangalore**
* **CSS Corp (Networking)**